CLAIMS

What is claimed is:

1. A memory comprising:

a plurality of parallel, spaced-apart silicon lines disposed on an oxide layer;

a plurality of parallel, spaced-apart conductive lines, generally perpendicular to the silicon lines disposed on the oxide layer, the conductive lines being non-continuous at intersections of the silicon lines, each intersection forming a body region in the silicon line and a first gate and a second gate on opposite sides of the body region formed from the conductive lines, the gate being insulated from the body regions; and

the first gates being coupled to word lines in the memory, and the second gates being coupled for biasing the body regions.

2. The memory defined by claim 1, wherein the body regions are doped with a first conductivity type dopant, and the silicon lines between the body regions forming source and drain regions which are doped with a second conductivity type dopant, the drain regions being coupled to bit lines in the memory.

3. The memory defined by claim 1, wherein the second gates in two adjacent ones of the conductive lines are connected together in a first overlying metal layer by a bridge, and wherein a plurality of such bridges are connected together by a biasing line in a second overlying metal layer.

4. The memory defined by claim 2, wherein the source regions are coupled to ground potential.

5. The memory defined by claim 4, wherein the biasing of the body regions by the second gates comprises coupling the second gates to a negative potential.

6. The memory defined by claim 1, wherein the conductive lines comprise polysilicon.

7. The memory defined by claim 6, wherein spacers are disposed along vertical sides of the conductive lines.

8. The memory defined by claim 1, including peripheral circuits formed on a common substrate with the memory.

9. The memory defined by claim 2, wherein the first conductivity type is p type and the second conductivity type is n type.

10. The memory defined by claim 1, wherein each body region provides storage for charge for a memory cell, and wherein adjacent memory cells share source regions, drain regions, first gates and second gates.

11. A dynamic random access memory cell in a memory array comprising:

a silicon member disposed on an insulative layer;

first and second spaced-apart, doped regions in the silicon member defining a body region therebetween;

first and second gates formed on the insulative layer, the gates being insulated from and being disposed on opposite sides of the body region;

a word line coupled to the first gate;

a bit line coupled to one of the doped regions.

12. The cell defined by claim 11, wherein the gates comprise polysilicon.

13. The cell defined by claim 12, including spacers formed on sides of the gates.

14. The cell defined by claim 13, wherein the doped regions are n type regions.

15. The cell defined by claim 14, wherein the second gate is coupled to a source of biasing.

16. The cell defined by claim 15, wherein the biasing source provides a negative potential to the second gate with respect to the other of the doped regions.

17. A method of fabricating a memory comprising:

forming a plurality of generally parallel, spaced-apart silicon lines on an insulative layer;

forming on the insulative layer, a plurality of generally parallel, spaced-apart conductive lines perpendicular to the plurality of silicon lines from a conductive material, such that the conductive lines are interrupted when intersecting the silicon lines, the conductive lines forming first and second gates on opposite sides of the silicon lines;

doping the silicon lines between the intersections so as to define source and drain regions separated by body regions;

connecting the first gates to word lines; and

connecting the drain regions to bit lines.

18. The method defined by claim 17, wherein the formation of the source and drain regions comprises, implanting the source and drain regions with a first conductivity type dopant, forming spacers on the sides of the conductive lines and again, doping the source and drain regions with the first conductivity type dopant such that the spacers block portions of the source and drain regions.

19. The method defined by claim 18, including the formation of a salicide on the source and drain regions.

20. The method defined by claim 17, wherein the conductive material comprises polysilicon.

21. The method defined by claim 17, including electrically pairing the second gates with overlying metal bridges and first contacts which extend between the second gates and the bridges.

22. The method defined by claim 21, including connecting the bridges to metal lines overlying the bridges with second contacts extending from approximately midway between ends of the bridges and the metal lines.

23. A memory comprising:

an array of cells, the cells having first gate contacts, second gate contacts, source region contacts and drain region contacts;

overlying metal bridges connected between pairs of the second gate contacts in an overlying metal layer; and

additional contacts contacting the bridges and connecting them to lines in another overlying metal layer.

24. The memory defined by claim 23, wherein the first gate contacts are connected to word lines in the array.

25. The memory defined by claim 24, wherein the drain region contacts are connected to bit lines in the array.

26. A memory comprising:

an array of cells, the cells having first gate contacts, second gate contacts, source region contacts and drain region contacts; and

the second gate contacts being coupled to lines in a first layer of metalization, the source region contacts and first gate contacts being coupled to lines in a second layer of metalization and the drain region contacts being coupled to lines in a third layer of metalization.

27. The memory defined by claim 26, wherein wherein the lines in the first and third layers of metalization are parallel to one another.

28. The memory defined by claim 27, wherein the lines in the second layer of metalization are perpendicular to the lines in the first and third layers of metalization.